What is claimed is:

1. A Flash memory comprising:

a plurality of array planes that constitute all storage corresponding to a logical address space the Flash memory device, each array plane including a plurality of blocks of memory cells, wherein the blocks have uniform size;

a write data path connected to the array planes; and

a read data path connected to the array planes, wherein the read data path is separate from the write data path and connected to permit a read operation in any one of the array planes while another of the array planes performs a write operation.

2. The Flash memory of claim 1, wherein the Flash memory stores data and parameters, and the uniform size of the blocks of memory cells corresponds to a unit of the parameters.

3. The Flash memory of claim 1, further comprising:

a content addressable memory array coupled to receive a logical address signal from an external device for comparison with defect addresses stored in the content addressable memory array;

a memory array having word lines coupled to respective match lines of the content addressable memory array, wherein in response to activation of one of the match lines, the memory array outputs a substitute address signal representing a substitute address stored in a row corresponding to the activated match line; and

multiplexing circuitry connected to select between the logical address signal and the substitute address signal as a physical address signal, the multiplexing circuitry providing the physical address signal to the plurality of array planes for selection of a memory cell being accessed.

4. The Flash memory of claim 3, wherein the blocks have physical addresses

corresponding to logical addresses from the external device, and each array plane further comprises a spare block having a physical address that does not correspond to a logical address from the external device.

5. The Flash memory of clam 4, wherein each array plane further comprises a spare global bit lines having a physical column address that does not correspond to a logical column address from the external device.

6. The Flash memory of clam 3, wherein each array plane further comprises a spare global bit lines having a physical column address that does not correspond to a logical column address from the external device.

7. The Flash memory of claim 3, wherein the memory array comprises a ROM array.

8. The Flash memory of claim 3, further comprising a set of Flash memory cells connected to the CAM array, the set of Flash memory cells containing the defect addresses that are loaded into the CAM array.

9. The Flash memory of claim 3, wherein the memory array comprises a RAM array.

10. The Flash memory of claim 9, further comprising:
a first set of Flash memory cells connected to the CAM array, the first set of Flash memory cells containing the defect addresses that are loaded from the first set into the CAM array; and
a second set of Flash memory cells connected to the RAM array, the second set of Flash memory cells containing the substitute addresses that are loaded from the second set into the RAM array.

11. The Flash memory of claim 1, wherein the blocks have physical addresses

corresponding to the logical address space, and each array plane further comprises a spare block having a physical address that does not correspond to the logical address space.

12. A Flash memory comprising:

memory elements having respective physical addresses that correspond to logical addresses of the Flash memory;

spare memory elements having respective physical address that do not correspond to the logical addresses of the Flash memory;

a content addressable memory array coupled to receive a logical address signal from an external device for comparison with defect addresses stored in the content addressable memory array;

a memory array having word lines coupled to respective match lines of the content addressable memory array, wherein in response to activation of one of the match lines, the memory array outputs a substitute address signal representing a substitute address stored in a row corresponding to the activated match line; and

multiplexing circuitry connected to select between the logical address signal and the substitute address signal as a physical address signal, the multiplexing circuitry providing the physical address signal for selection of a memory cell being accessed.

13. The memory of claim 12, wherein each memory element and each spare memory element is a block of memory cells that are connected to permit simultaneous erasure of all of the memory cells in the block.

14. The memory of claim 13, further comprising:

a write data path; and

a read data path, wherein

the blocks are organized into a plurality of array planes, the array planes being connected to the write and read data path so as to permit any one of the array planes to conduct a read operation while any other of the array planes conducts a write operation.

15. The memory of claim 14, wherein each array plane contains erase circuit that permits the array plane to erase a block in the array plane, while other array planes conduct read and write operations.

16. The memory of claim 14, wherein each array plane comprises at least one of the spare memory elements.

17. The memory of claim 16, wherein each array plane comprises a spare global bit line that connects to all blocks in the array plane.

18. An operating method for a Flash memory, comprising:
storing defect addresses in a content addressable memory array in the Flash memory;
storing substitute addresses in a memory array in the Flash memory;
applying a first logical address from an external device to the content addressable memory array for a comparison operation;
outputting from the memory array a substitute address corresponding to a match line activated as a result of the comparison operation; and
accessing a memory element corresponding to the substitute address instead of a memory element corresponding to the first logical address.

19. The method of claim 18, further comprising applying a second logical address from the external device directly to a decoder in the Flash memory while applying the first logical address to the content addressable memory, wherein a combination of the first and second logical addresses identifies a memory cell.

20. The method of claim 19, wherein the first logical address is a block address and the second logical address identifies a memory cell within a block.

21. The method of claim 20, wherein the second logical address is a row address.

22. The method of claim 18, wherein accessing the memory element comprises accessing a first array plane in the Flash memory while a second array plane in the Flash memory conducts a second operation.

23. The method of claim 22, wherein accessing the first array plane comprises reading a memory cell in the first array plane, and the second operation comprises writing to a memory cell in the second array plane.

24. The method of claim 22, wherein accessing the first array plane comprises reading a memory cell in the first array plane, and the second operation comprises erasing a block in the second array plane.

25. A method for operating a Flash memory, comprising:
performing a write operation in a first array plane in the Flash memory;
performing a read operation in a second array plane in the Flash memory; and
performing an erase operation in a third array plane in the Flash memory, wherein for a period of time, the erase operation, the read operation, and the write operation are simultaneously being performed.

26. The method of claim 25, further comprising:
providing data to the first array plane for the write operation via a write data path that is connected to all of the array planes; and
output data read from the second array via a read data path that is connected to all of the array planes, wherein
the erase operation does not require use of the write data path or the read data path.